Model 8706
Analog-to-Digital-Converter

Features

- 450 MHz Wilkinson ADC
- 16K channel resolution
- Digital offset in 256 channel increments
- Exceptional linearity (differential <± 0.7%, integral <± 0.025%)
- Pulse height analysis using either automatic peak detection or delayed triggering
- Analog sample voltage analysis
- Pulse pileup rejection and live time correction interfaces
- Compatible with Loss Free Counting Systems[1]

Description

The Model 8706 Wilkinson analog-to-digital converter is designed for high resolution nuclear spectroscopy. Its 450 MHz counter/ramp-converter is optimized to provide high resolution performance at medium to high throughput rates. Its exceptional linearity improves your peak shapes and resolution, thereby improving the overall performance of your spectroscopy system.

The 8706's fast clock rate allows it to digitize a full scale input pulse (with an 8K conversion gain setting) in less than 19 µs and in statistical applications such as spectroscopy, the average conversion time is less than 6.1 µs. The ADC also includes an internal data buffer which allows it to begin a second conversion prior to MCA acceptance of the first, further enhancing throughput.

Concentric Gain and Range controls together with digital Offset allow the user to maximize the use of limited MCA memory by selecting only a specific energy range of interest. This can be particularly useful for multi input applications such as alpha spectroscopy, thus eliminating the need for older biased amplifiers. These digital controls accomplish the same end more accurately and repeatably.

Conversion for the Pulse Height Analysis (PHA) mode can be initiated Automatically using an internal constant-fraction peak detector operating on the trailing edge of the input pulse, or can be Delayed up to 100 µs after the leading edge of the input pulse passes the input threshold. A front panel Inspect test point is provided for monitoring the Linear Gate (LG), the time between the input threshold crossing and the beginning of conversion for either mode. Conversions may be enabled/disabled by Coincidence/Anticoincidence gating applied at any time during the Linear Gate Interval.

Conversion for the Sampled Voltage Analysis mode is initiated by the falling edge of a Gate pulse applied in the Coincidence mode. The same LLD and ULD limits are used for acceptance of the peak input during the positive gate time. The 8706 provides front panel screwdriver-adjustable, multi-turn, potentiometers for the control of the Lower and Upper Level Discriminators as well as for the ADC Zero.

The 8706 provides the connections required for use with current Canberra amplifiers that perform pileup rejection and live time correction (PUR/LTC). These ADC/amplifier interfaces are also required to use the Westphal loss free counting or precision live time techniques.[2]

1. US patent 4,476,384.
2. G. P. Westphal, Nuclear Instruments and Methods 163 (1979) 189-196.

The 8706 ADC is fully compatible with all current Canberra MCAs (with external ADC interface options), Digital Stabilizer and Analog Multiplexers.

Specifications

INPUTS

ADC IN - Accepts positive unipolar or bipolar (positive lobe leading) pulses for PHA, and dc level or pulses for the SVA mode; amplitude 0 to +10 V, +12 V maximum; rise time 0.25 to 100 µs maximum; width 0.5 µs minimum; Z_{in} 1 kΩ, direct coupled; front panel BNC and test point.

GATE IN - Accepts a positive logic pulse or dc level; high amplitude ≥+2.5, Low amplitude ≤400 mV, 0 to +7 V maximum; dc coupled; Loading with COINCidence selected is 27 kΩ to +5 V and 27 kΩ to −12 V for ANTIcoincidence; width ≥250 ns; PHA analysis does not require a gate input; minimum gate pulse width for SVA is 1 µs.

DEAD TIME - Rear panel BNC connector which receives an external dead time INPUT. Accepts a negative or positive logic signal, jumper selectable, which is ORed with the ADC dead time; negative true amplitude ≤400 mV, positive true amplitude ≥+2.5 V, 0 to +7 V maximum; loading 4.7 kΩ to +5 V. The composite dead time signal may be accessed through pin 6 of the rear panel DATA connector. Internal jumper plug selects the output composite dead time signal polarity, positive true or negative true; shipped in the NEG position; TTL compatible with 4.7 kΩ pull-up resistor.

OUTPUTS

DATA - Provides 14 binary TTL-compatible output lines and the data transfer commands required for MCA interface; rear panel 34-pin ribbon cable connector. Data lines are negative true. Two input lines are also provided for the Model 8233 Digital Stabilizer correction voltages. Stabilizer Control range; zero: ±2%, gain: ±5%.

PILEUP REJECTOR/LIVE TIME CORRECTOR - Accepts Reject and Live Time signals from Canberra amplifiers equipped with PUR/LTC. It also provides Linear Gate to those units for full interactive operation; rear panel 3-pin Molex connector for use with Model C1514 PUR/LTC interface cable.

REJect - Receives a positive true logic pulse used to initiate an ADC reject sequence; must occur during the ADC Linear Gate (LG) signal time; amplitude ≥2.5, 0 to 7 V maximum; width ≥100 ns; loading ≥2 kΩ to −12 V. Accessible through pin 2 of the rear panel PUR connector.

LG - Provides a negative true logic signal; logic low while the ADC acquires an input pulse, returns to a logic high at the pulse acquisition conclusion. TTL compatible output, 47 Ω series resistor. Accessible through pin 1 of the rear panel PUR connector. The LG signal may be viewed on the front panel INSPect test point, positive true, series 220 Ω resistor.

FRONT PANEL CONTROLS

GAIN - Six-position rotary switch to select full scale resolution of the input signal; selection of 512, 1024, 2048, 4096, 8192, or 16 384 channels for a 10 V input pulse or level.

RANGE - Six-position rotary switch to select 512, 1024, 2048, 4096, 8192, or 16 384 channels as the upper output address limit.

OFFSET - Six toggle switches to digitally offset the spectrum to the left; subtracts 0 to 16 128 channels in binary multiples of 256 channels.

LLD - Screwdriver-adjusted multi-turn potentiometer sets the Lower Level Discriminator for minimum input acceptance voltage; range +0.02 V to +10 V dc. The input threshold tracks the LLD to 100 mV.

ULD - Screwdriver-adjusted multi-turn potentiometer sets the Upper Level Discriminator for maximum input acceptance voltage; range +0.02 V to +10.5 V dc.

ZERO - Screwdriver-adjusted multi-turn potentiometer sets the input analog zero level; adjustment range ±5% of the ADC full scale range.

PEAK DETECT - Toggle switch to select either AUTOmatic or DELAYED initiation of conversion cycle. In AUTOmatic an internal constant-fraction trigger operates on the falling edge of the input pulse. In DELAYED mode, the conversion begins after a user selectable delay, initiated by the input signal rising through the input threshold setting. An ADJustment potentiometer permits selection of a delay from 2 to 100 µs. An INSPect test point is provided to monitor the Linear Gate time delay adjustment, positive true, series 220 Ω resistor.

COINC/ANTI - Toggle switch to select either the COINCidence or the ANTIcoincidence gating mode. In the COINCidence mode (ANTIcoincidence) a positive GATE pulse enables (disables) the conversion of the present input. If gating is used, the pulse must be present during the Linear Gate time as monitored on the INSPect test point.

PHA/SVA - Toggle switch to select the Pulse Height or Sampled Voltage Analysis mode. In PHA, the conversion cycle is initiated by the INPUT pulse. In SVA, the conversion cycle is initiated by a GATE pulse. In either mode, the LLD and ULD acceptance criteria apply.

The GATE pulse must be positive in COINC mode or inverted in ANTI mode.

INDICATORS

DEAD TIME - 20 segment LED indicator displays the average dead time of the converter.

PERFORMANCE

INTEGRAL NONLINEARITY - <±0.025% of full scale over the top 99.5% of selected range.

DIFFERENTIAL NONLINEARITY - <±0.7% over the top 99.5% of range including effects from integral nonlinearity.

GAIN DRIFT - <±0.009% of full scale/°C

ZERO DRIFT - <±0.0025% of full scale/°C

LONG TERM DRIFT - <±0.005% of full scale/24 hours at a constant temperature.

PEAK SHIFT - <±0.025 of full scale at rates up to 100 kHz.

ADC DEAD TIME - Linear Gate Time + Conversion Time.

CONVERSION TIME - 0.7 µs +0.0022 (N + X) µs where N = address count, and X = effective digital OFFSET.

CHANNEL PROFILE - Typically flat over 90% of channel width.

POWER REQUIREMENTS

+24 V - 75 mA	+12 V - 250 mA
−24 V - 75 mA	−12 V - 250 mA

PHYSICAL

SIZE - Standard single width NIM module 3.42 x 22.12 cm (1.35 x 8.71 in.) per DOE/ER-00457T

NET WEIGHT - 0.9 kg (1.9 lb)

SHIPPING WEIGHT - 1.8 kg (4.0 lb)

CABLES

Cable not supplied; MCA must support 34-pin ADC Standard. Consult factory if required.