LeCroy

RESEARCH SYSTEMS

CAMAC MODEL 2264

MULTICHANNEL WAVEFORM DIGITIZER

innovators in instrumentation

SPRING VALLEY, N.Y.

technical information manual

CAMAC MODEL 2264

MULTICHANNEL WAVEFORM DIGITIZER

WARRANTY

All LRS instruments are guaranteed to operate within their specifications for one year from the date of purchase. Under this warranty, any unit which fails to perform within specifications, as a result of defects in workmanship or materials, will be restored to specified operating condition free of charge except for shipping costs involved in the return of the unit to the factory.

In order that this warranty be considered valid, it is necessary that the LRS Warranty Card which accompanies the unit on delivery be completed and returned to the factory within 30 days of receipt of equipment.

All questions concerning repairs or replacement parts should be addressed directly to factory's Quality Control Manager. This procedure will insure the fastest possible service. Please include the Model Type, Serial Number, and ECN (Engineering Change Number) with all requests for parts or service.

ENGINEERING DEPARTMENT
LeCroy Research Systems Corp.

November 1977

NOTE TO THE USER

LeCroy Research Systems is committed to providing unique,reliable, state-of-the-art instrumentation in the field of high-speed data acquisition and processing. Because of this commitment, and in response to information received from the users of our equipment, the Engineering Department at LeCroy is continually seeking to refine and improve the performance of our products.

While the actual physical modifications or changes necessary to improve a model's operation can be implemented quite rapidly, the corrected documentation associated with the unit usually requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying unit. There may be small discrepancies that were brought about by customer-prompted engineering changes or by changes determined during calibration in our Test Department. These differences usually are changes in the values of components for the purposes of pulse shape, timing, offset, etc., and only rarely include minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry. Whenever original discrepancies exist, fully updated documentation should be available upon your request within a month after your receipt of the unit.

If you have any questions about the performance or operation of this unit, rapid assistance may be obtained from our Engineering Services Department in Palo Alto, CA, telephone 415-328-3750, or from your local distributor in countries other than the U.S.A.

LeCROY RESEARCH SYSTEMS

The LeCroy ADC employed in this module is truly unique in its capability to precisely track high frequency waveforms. The extremely low aperture uncertainty and high ADC bandwidth requires precise maintenance of calibration. For this reason, LeCroy does not recommend field servicing of this board. Any problems associated with the ADC board will require shipment back to LeCroy/California or your local LeCroy service facility for diagnostic evaluation and correction. Specially designed diagnostic equipment is necessary to repair and calibrate the ADC board such that critical instrument specifications will be maintained. Therefore, only a block diagram of the ADC board is included in this manual.

Evidence of any attempt at field-servicing the ADC board will void the warranty and will necessitate specific charges for repair and recalibration.

Field-servicing can be performed on the digital board without voiding the warranty. Schematics are provided for this purpose.

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TECHNICAL DATA

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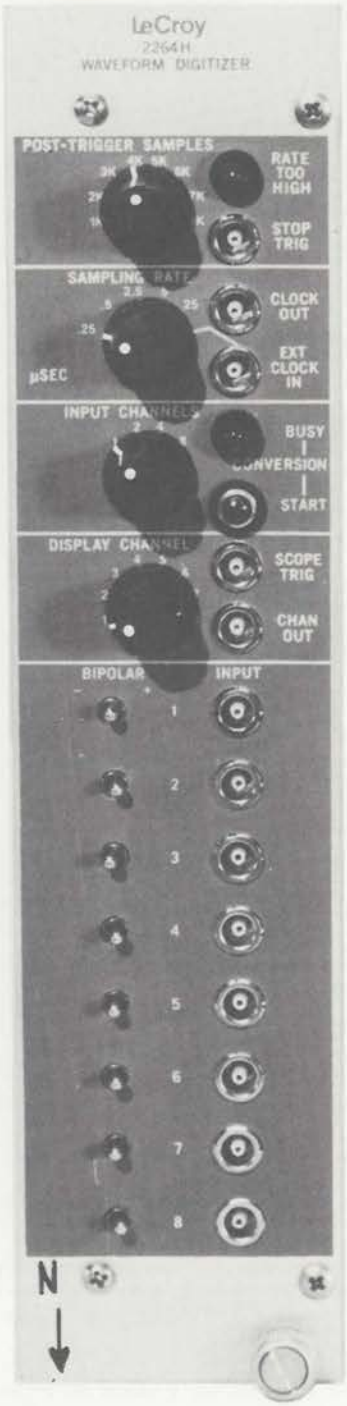

CAMAC Model 2264

Multichannel Waveform Digitizer

FEATURES:

* **1, 2, 4 or 8 input channels**
* **Eight bits of dynamic range and resolution**
* **500 kHz maximum sampling rate (4 MHz in single-channel mode)**
* **150 picosecond sample time uncertainty; 1 MHz analog bandwidth**
* **Inputs fully protected with good overload recovery**
* **Companion memory expandable in 32 K word steps**
* **High sensitivity of 2 mV/count, maximum**
* **3-level input offset for each channel**
* **Excellent interchannel crosstalk isolation**
* **Analog readout of memory viewable on any scope**
* **Non-destructive readout by standard CAMAC commands**
* **Low-cost per channel with high flexibility of use**

The LeCroy Multichannel Waveform Digitizer is the second in a developing line of modularized transient recording systems packaged according to the international CAMAC standard. The Model 2264 ADC employs an analog multiplexer and a high-speed 8-bit digitizer. Up to 8 input signals are sampled at rates as high as 4 MHz and transferred to a Model 8800/8 memory with a capacity of 32 K 8-bit words. Up to 4 of these modules can be used with one Model 2264, giving a capacity of 128 K 8-bit words. Further memory extension is possible as a factory option. The memory design allows the Model 8800 Series to be used in other LeCroy transient recording systems—for instance, with a 12-bit analog-to-digital converter (8800/12) or as a part of a 20 MHz Video Digitizer (8800/9).

The data is read out through the Model 2264 and reorganized to place all samples from a particular channel together. Readout is non-destructive, and a DAC display is provided for presentation on any scope.

The flexibility of the design concept also allows the external clock frequency to be varied with time, permitting "importance" sampling along a single waveform. The "burst mode" channel multiplexing yields relatively simultaneous sampling with the economy and flexibility of a multiplexed single ADC approach.

The system digitizes continuously, which allows retention of waveform data recorded before the stop trigger. This presampling capability allows recording the baseline value previous to the occurrence of the meaningful signal, for instance.

Packaged in a #3 width CAMAC module, the Model 2264 gives high function density at a reasonable price while maintaining superior specifications. All integrated circuits are socketed, and the circuit boards are hinged for easy maintenance.

September 1977

Instrumentation for the study of transient phenomena

LeCROY RESEARCH SYSTEMS OF CALIFORNIA • 1806 Embarcadero Rd. • Palo Alto, California 94303
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SPECIFICATIONS
CAMAC Model 2264
MULTICHANNEL WAVEFORM DIGITIZER

INPUT CHARACTERISTICS

Number of Inputs:	1, 2, 4 or 8; switch-selectable.
Impedance:	50 Ω (up to 100 kΩ at a reduced bandwidth—Model 2264H).
Full Scale Amplitude Range:	512 mV. Each input can separately accept negative, positive, or bipolar signals. In the bipolar mode, maximum signal amplitude is 256 mV (10.24 volt range available—Model 2264H).
Overvoltage Protection:	Input protected against ±5 A transients for 0.5 μsec clamping at ±1 volt.
Input Analog 3 dB Bandwidth:	1 MHz for all configurations (≥100 kHz for 100 kΩ input impedance—Model 2264H).
System Aperture Uncertainty:	<150 psec, defined as the uncertainty in the actual sample-taking time relative to the leading edge of the clock. This corresponds to an upper limit of 2 MHz on the frequency of the sinusoidal wave which can be reconstructed with 8-bit accuracy from the ADC.
Integral Linearity:	Better than 0.5% of full scale.

WAVEFORM SAMPLING ORGANIZATION

Sampling Rate:	DC to a maximum of 4 MHz for 1 input, 2 MHz for 2 inputs, 1 MHz for 3, 4, inputs, and 0.5 MHz for 5, 6, 7, 8 inputs. Front-panel LED blinks for improper combinations of sampling and number of channels.
Internal Clock:	Front-panel selectable from 40 kHz to 4 MHz. Stability, ±0.01%. The internal clock is available for synchronization purposes at a front-panel LEMO connector.
External Clock Input:	One LEMO-type connector, 50 Ω input impedance; required TTL level pulses; valid frequency range 0 to the maximum frequency given by the number of active channels. The external clock can be varied in frequency to achieve importance sampling.
Burst Mode Multiplexing:	Once a clock pulse leading edge triggers the sampling circuit, an internally generated clock samples all active inputs 200 nsec apart during the clock period.
Digitizing:	A very fast track and hold circuit eliminates all slewing problems in the comparator-based digitizing circuitry. The tracking and digitizing accuracy is 8-bits (1 part in 256 or 0.4%).
Memory Organization:	The memory is contained in separate modules, each capable of storing up to 32,000 12-bit words. (See further description of LeCroy Model 8800/8)

READOUT METHODS

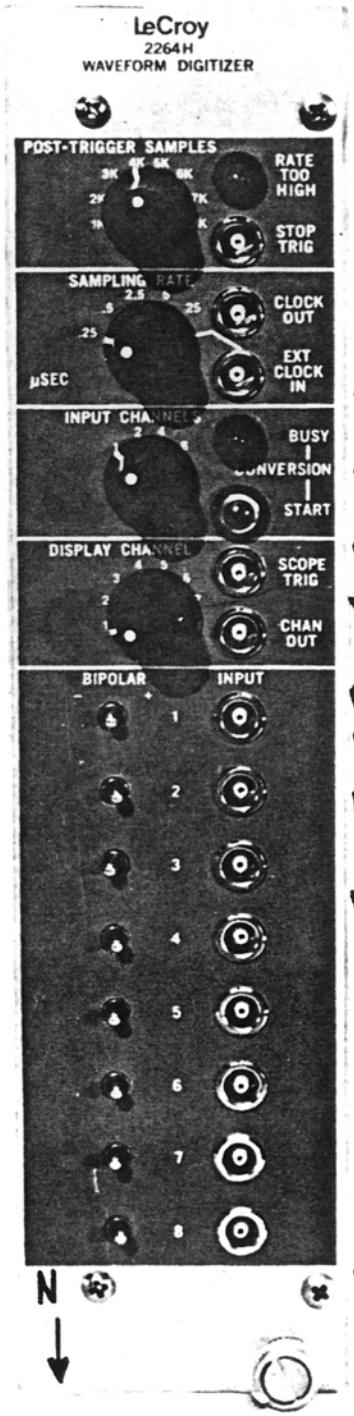
Display:	A built-in display driver allows the memory contents of a selected input channel to be viewed on any real time oscilloscope. After a conversion cycle is completed, the Model 2264 supplies a display signal at a refresh rate depending upon the total memory size. Each sweep consists of a separate negative sync signal for trigger purposes and a waveform proportional to the amplitude of the input signal. A rotary switch selects the channel to be displayed. The time base and delayed sweep features of most laboratory oscilloscopes allow either the entire waveform or a segment of the waveform to be viewed.
Computer Readout:	Once a conversion cycle has been completed, the data can be read two words at a time at the fastest rate permitted by the CAMAC standard. (See the following CAMAC commands for a detailed description of the readout). Separate CAMAC commands read the status of the front-panel switches. Word count and Q switching DMA's are possible.
CAMAC Commands:	*L*: In order to generate a Look-At-Me signal, the DAC display must be disabled. This is done by enabling the LAM with a F(26) command. After the DAC has cycled through the rest of the memory (less than 20 msec latency period), a Look-At-Me signal is generated to indicate that the module is ready to be read out. *Q*: A Q=1 response is generated in recognition of a F(2)•N only, when a valid word is being read. After all data has been read for a given input channel or pair of channels, the next readout will generate a Q=0 response. The size of the memory, which depends upon the number of expandable memory modules used, is programmed into the Model 2264 by a jumper option. *Z*: The continuous sampling cycle is re-initiated; requires S2; LAM enable is reset. *C*: Same effect as Z. *X*: An X=1 (Command Accepted) response is generated when a valid F and N are generated.
CAMAC Function Codes:	*F (0)*: Reads out front-panel offset switches, with 2-bits of information for each of the 8 switches. R1 and R2 are assigned to Channel 1 and further bits are assigned in ascending order up to R15 and R16 for Channel 8. The coding is as follows: 11 - 0 offset (bipolar) 01 - negative pulses 10 - positive pulses *F (1)*: Reads out remaining front-panel switches as follows: Pretrigger samples in multiples of 1,024 words binarily encoded on R1, R2, R3. Internal clock frequency is encoded on R4, R5, R6. Number of active channels are coded on R7 and R8 corresponding to the four possibilities, 1, 2, 4 or 8. Dropped Word Flag: Due to the dual word readout technique, if the unit is used in the single-channel mode, an odd number of samples taken after the trigger can result in the truncation of a single word of data. If that has been done, this flag is raised. (R(9)). Incompatible Switch Flag: R(10) is set if combination of sampling rate and number of channels is not allowed. *F (2)*: Read data registers. Requires N and S2. Successive F(2)•N commands will read successive 16-bit words from memory. 16-bit words correspond to two words of data, either the same sample of adjacent channels or successive samples of Channel 1. *F(8)*: Test LAM. Requires N and an A(0). Q response is generated if LAM is set. *F(9)*: Clear control register and reset the LAM enable and initiate continuous sampling cycle. Requires N and S2. *F(10)*: Clear LAM. Requires N, S2 and A(0). *F(16)*: Select channel to be read. Combination of front-panel switch position and the sub-address lines determines the channel, or channels, to be read out as below: (Requires N, S1, and S2.) *1 Channel selected* on input channels switch: F(16)•A(0) causes subsequent F(2)•N commands to read out channel 1, with the lower 8 bits containing the first sample and the upper 8 bits containing the second sample. *2 Channels selected* on input channels switch: F(16)•A(0) causes subsequent F(2)•N commands to read samples from channels 1 and 2 in the lower and upper 8 bit half words respectively. *4 Channels* selected on input channels switch: F(16)•A(0) causes subsequent F(2)•N commands to read samples from channels 1 and 2 in the lower and upper 8-bit half words respectively. F(16)•A(2) will then set up the readout of channels 3 and 4 in the lower and upper half words, to be transferred upon receipt of F(2)•N commands. *8 Channels selected* on input channels switch: F(16)•A(0), or F(16)•A(1), or F(16•A(2) or F(16•A(3) causes subsequent F(2)•N commands to read out (1 and 2) or (3 and 4) or (5 and 6) or (7 and 8) respectively in a manner similar to above. *F(24)*: Disable Look-At-Me (LAM)= requires N, S2 and A(0). This command will initiate the DAC display and reset subsequent CAMAC readout to the earliest sample taken. *F(25)*: Provides a "Stop Trigger" via the Dataway. May be used as a test function between events. *F(26)*: Enable LAM and stop DAC display. This command is necessary for any computer readout of the module. There may be as much as 20 msec latency period to allow the DAC to cycle through the rest of the memory. (Caution: The state of the LAM mask is arbitrary after the power turn-on).

GENERAL

Interconnecting Cable:	To permit data transfer from the Model 2264 to the Model 8800/8 Memory Modules, a Model DC8800/n Data Cable is required, where "n" equals the number of memory modules linked to the 2264.
Packaging:	Conforms to the CAMAC standard for nuclear instrumentation modules (ESONE Committee Report EUR 4100e or IEEE Report #583).
Current Requirement:	+6 volts at 1.50 A −6 volts at 250 mA +24 volts at 100 mA −24 volts at 50 mA

CAMAC Model 2264, H

Multichannel Waveform Digitizer



(LED lights if combination of sampling rate
(and number of channels is inconsistent.

(Switch selects number of samples taken
(after the stop trigger

(TTL level pulse initiates post trigger
(run down scaler

(Switch selects number of microseconds
(between samples.

(Drives 50 ohm load to TTL level at the
(internal clock sampling rate.

(Leading edge of TTL pulse causes unit to
(take a sample in all channels.

(Switch selects number of input channels
(and determines highest possible frequency.

LED lights when unit is digitizing

Manual pushbutton initiates sampling.

Switch selects channel to be displayed.

(Separate scope trigger allows manipulation
(of scope gain, time base, etc. without
(losing trigger.

(Display output proportional to input
(signal at a flicker free refresh rate

Individual Inputs 50 ohm impedance
(100K ohm in the H option)

(Individual DC level offsets
(- for negative signals
(bipolar for both signs
(+ for positive signals

CAMAC #3 Module. Addressable slot is
the left most.

ENGINEERING DEPARTMENT
LeCroy Research Systems Corp.
Palo Alto, California

3. ADDENDA TO SPECIFICATIONS

Memory Organization:	The memory is contained in separate modules, each capable of storing up to 32,768 12-bit words.....
Display:	.....Each sweep consists of a separate positive sync signal for trigger purposes and a waveform proportional to the amplitude of the input signal. .....
Computer Readout:	Once a conversion cycle has been completed, the data can be read two words at a time (See the following CAMAC commands for a detailed description of the readout).....
CAMAC Function Codes:	4 Channels selected on input channels switch:..... F(16)·A(1) will then set up the readout of channels 3 and 4 in the lower and upper half words.....
Current Requirement:	+6 volts at 1.9 A -6 volts at 2.1 A +24 volts at 200 mA -24 volts at 75 mA

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4. OPERATIONAL DESCRIPTION

4a. General

The LeCroy Model 2264 Multichannel Waveform Digitizer is an eight bit analog to digital converter which can process signals from up to 8 different sources through a programmable multiplexer. The maximum sampling rate per channel is 4 MHz in the single channel mode; 2 MHz in the two channel mode; 1 MHz in the four channel mode; 0.5 MHz in the eight channel mode.

The sampling and ADC conversions are controlled by a 5 MHz burst clock. In the multichannel modes, samples from successive input channels are multiplexed into the ADC at 200 nsec intervals regardless of the sampling rate per channel which is controlled by the internal, front panel programmable, master clock or an external clock signal provided by the user.

The A/D conversion for each sample is effected by two consecutive 4 bit flash comparisons. The first comparison yields the upper four bits (2^7 to 2^4). These bits are then reconverted to an analog signal which is subtracted from the original input analog signal. The remaining signal is then fed to the second flash converter which yields the least significant four bits ($2^3 - 2^0$). The digital data is then directed by internal circuitry to the 2264 output connector along with timing and control signals appropriate for interfacing with LeCroy Model 8800/8 cascadable memory modules. This allows the data to be stored in a memory of up to 128K, 8 bit words in 32K increments.

The Model 2264 also contains circuitry which sequentially reads the memory and sorts the data such that the digital data for any selected channel can be placed on the CAMAC dataway or reconverted to analog form by an internal DAC for viewing on an external scope.

Front Panel Inputs, Controls and Indicators

Analog Inputs: Eight LEMO type input connectors. Input impedance 50 Ω (100K Ω for Model 2264H), bandwidth greater than 1 MHz (100 kHz for Model 2264H). Full scale amplitude range is 512 mV (10.24 mV for Model 2264H).

Offset Switches: A 3-position offset switch adjacent to each input connector permits setting the offset of the input amplifier to -0.256 V, 0 V, or +0.256 V (-5.12 V, 0 V, or +5.12 V for Model 2264H). The full input amplitude range may then be used for ground referenced positive, bipolar or negative input signals. For negative unipolar signals the switch should be placed in the "-" position, for bipolar signals in the center position, and for positive unipolar signals in the "+" position. The offset switch settings may be read out as a digital code on the CAMAC dataway. (See Table II in

CAMAC Control Section.)

Sampling Period Switch: The sampling period per channel may be internally set to the rates indicated at the first five positions of the switch 0.25, 0.5, 2.5, 5 and 25 μsec. When the switch is in the Ext. Clk. position, the sampling period is determined by the frequency of the external clock.

External Clock Input: Allows user to determine sampling rate per channel by input from a TTL level clock generator. Input Impedance is 50 Ω. The allowable external clock frequencies (also applies to internally selected clock rates) are indicated below:

No. of Channels Switch	Maximum Sample Rate/Channel
1	0 to 4 MHz
2	0 to 2 MHz
4	0 to 1 MHz
8	0 to 0.5 MHz

To allow for "importance sampling", the clock rate may vary over the allowable range provided the clock is free of anamalous trailing edges.

Rate Too High Indicator: When using the internal sampling clock, if an illegal combination of number of input channels and sampling period is selected, the LED near the top of the panel will blink.

No. of Input Channels Switch: Programs input multiplexer to switch signals to the ADC from channel one only in the 1 position, from channels one and two only in the 2 position, from channels one through four in the 4 position, and from all eight channels in the 8 position.

Conversion Start Button: Resets internal logic and starts continuous sample, convert, and store cycling.

Busy Indicator: LED adjacent to conversion start button lights during sample, convert and store operations, remains off during readout and display operations.

Stop Trigger Input: LEMO type connector, 50 Ω input impedance, requires positive going TTL pulse of at least 50 nsec duration. A proper trigger will stop the data conversion and storage process after the selected number of post-trigger samples have been taken.

Post-Trigger Samples Switch: The position of this switch controls the number of samples converted and stored per input channel following the stop trigger

pulse. The switch has positions 1 through 8. Normally the unit is programmed (wire jumpers) such that the numbers correspond to thousands of post-trigger samples, i.e., position 8 means 8K post-trigger samples per channel. The programming of the switch is done on a wire jumper platform.

Display Channel Switch: Digital data of selected channel is reconverted to an analog signal for display on a scope. The signal is available from the "channel out" connector.

* NOTE: During operation the display channel switch and post-trigger samples switch may be changed at any time but the other panel switches should be preset before a conversion is initiated and not changed until a new conversion-readout cycle is to be initiated under new conditions. The internal timing may be upset by changing these switches so that the logic must be reset by starting a new conversion cycle to restore the proper timing as determined by the settings of the switches.

4b. Front Panel Outputs

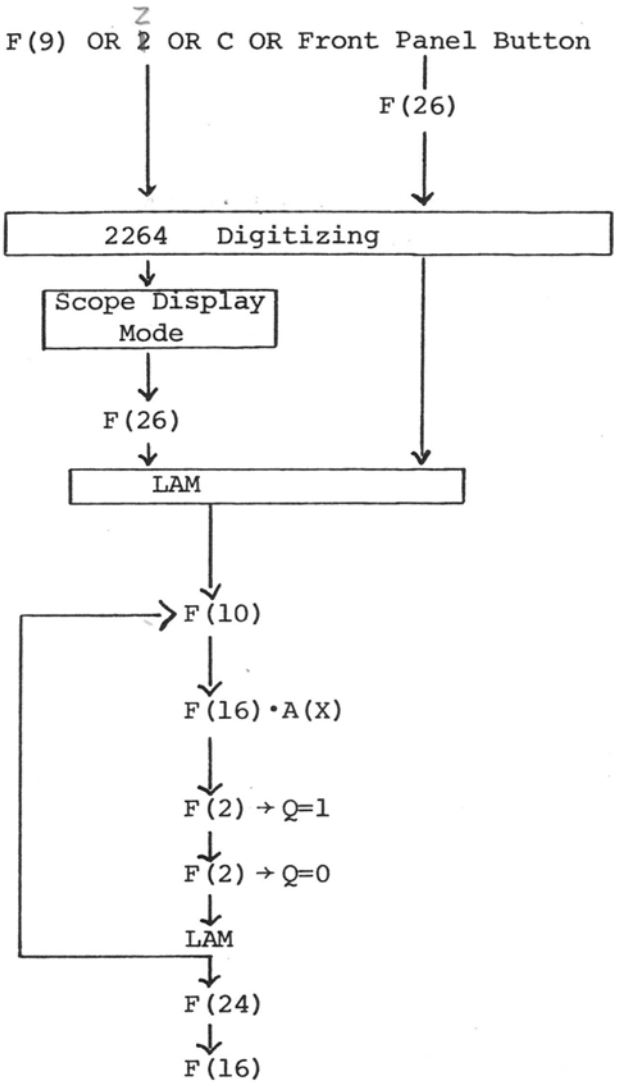
Internal Clock Out: Drives 50 Ω load to TTL levels. Permits synchronization of multiple 2264's by timing all sampling with respect to a single clock.

Channel Display Output: LEMO connector. After a stop-trigger and the selected number of post-trigger samples per channel has been digitized, the Model 2264 will enter the scope display output mode (unless the LAM is enabled - see CAMAC section). The data from any input channel may be displayed on an oscilloscope by setting the display channel switch to the desired channel number. The amplitude of the output signal into a high impedance scope input is between -2.5 volts and +2.5 volts (the scope display output should not be terminated). The data points are displayed at an approximate rate of 800 nsec per point in the one or two input channel mode, 1600 nsec per point in the four channel mode, and 2400 nsec per point in the eight channel mode. The scope sweep rate is set by the user to display the desired number of points.

NOTE: In the single channel mode, only every other data point will be displayed.

Scope Trigger Out: LEMO connector. A TTL positive going pulse occurring at the time the first data word is output for display. This pulse may drive the external trigger input of a scope so that the sweep will always start with the earliest data point. This output should not be terminated.

EXAMPLE OF 2264 CAMAC CONTROL SEQUENCE



- Initiate Sampling

F(26) — Enable LAM (only necessary if 2264 is to enter CAMAC readout made after conversion completed).

2264 Digitizing — Stop Trigger pulse OR F(25)

Scope Display Mode — 2264 enters scope display mode unless F(26) command was performed above.

LAM — 2264 ready for CAMAC readout (Read LAM or test for LAM by Q=1 in response to F(8)).

F(10) — Reset LAM

F(16)•A(X) — Select channel(s) to be readout (see Table I)

F(2) → Q=1 — READ DATA for selected channel(s).

F(2) → Q=0 — Readout complete

LAM

F(24) — Disable LAM

F(16) — Enable scope display.

NOTE: All CAMAC F(X) commands require N.

SELECTING CHANNELS FOR CAMAC READOUT

TABLE I

CAMAC Command	No. Of Channels Selected On Front Panel	Result
F(16) • A(0)	1	Select Channel No. 1 (n^{th} sample or R1 - R8, $(n+1)^{th}$ sample on R9 - R16)
F(16) • A(0)	2, 4 or 8	Select Channel no. 1 and #2 (channel 1 on R1 - R8, Channel 2 on R9 - R16).
F(16) • A(1)	4 or 8	Select channel no. 3 and no. 4 (channel 3 on R1 - R8, channel 4 on R9 - R16).
F(16) • A(2)	8	Select channel no. 5 and no. 6 (channel 5 on R1 - R8, channel 6 on R9 - R16).
F(16) • A(3)	8	Select channel no. 7 and no. 8 (channel 7 on R1 - R8, channel 8 on R9 - R16).

* NOTE: F(16) commands also require N, S1 and S2. DATA is output in a complementary binary code, i.e., the most positive voltage in the input voltage range is represented by all "zeros", and the most negative voltage in the input voltage range by all "ones".

CAMAC READOUT OF FRONT PANEL INFORMATION

TABLE II

A) N·F(0) reads the position of the front panel offset switches.

(a)

Channel Number	(Position of Code on R lines) 2^0	2^1
1	R1	R2
2	R3	R4
3	R5	R6
4	R7	R8
5	R9	R10
6	R11	R12
7	R13	R14
8	R15	R16

(b) Codes:

	2^0	2^1
Positive Offset	1	0
Zero Offset	1	1
Negative Offset	0	1

TABLE III

B) N·F(1) reads the setting of the post trigger samples switch, the sampling period switch, number of channels switch, odd/even samples flag,and rate too high flag.

(a) Post-Trigger Samples Switch Setting	2^0 R_1	2^1 R_2	2^2 R_3
8	0	0	0
7	1	0	0
6	0	1	0
5	1	1	0
4	0	0	1
3	1	0	1
2	0	1	1
1	1	1	1

(Code) (CAMAC R Lines)

(b) Sampling Period Switch Setting	2^0 R_4	2^1 R_5	2^2 R_6
Ext.	0	1	0
25 µsec	1	1	0
5 µsec	0	0	1
2.5 µsec	1	0	1
.5 µsec	0	1	1
.25 µsec	1	1	1

(c) No. of Channels Switch Settings	2^0 R_7	2^1 R_8
8	0	0
4	1	0
2	0	1
1	1	1

(d) ODD/EVEN Flag - If running in the single channel mode, the 2264 will truncate the last sample if it is to be stored in the first half of the 2800 memory. This condition is flagged on R9 during N·F(1).

R9=1: No Sample Truncated - Earliest sample = 64K - Post Trigger samples from trigger.

R9=0: One Sample Truncated - Earliest sample =(64K +1) - Post Trigger samples from trigger.

(e) When using the internal sampling clock, if an illegal combination of input channel number and sampling period is selected, the RATE TOO HIGH inidicator will blink, and a flag will be raised on R10 during N•F(1).

R10=1: Illegal switch settings.
R10=0: Switch settings legal.

5. FUNCTIONAL DESCRIPTION

5a. General

The Model 2264 is a multichannel waveform digitizer composed of an analog to digital converter (ADC) board and a controller board which includes the analog signal multiplexing circuits that feed the ADC and the digital circuits needed to control the storage of the digital data in Model 8800 memory modules. This board also contains the circuitry needed to read the data from the memory and either places the data on the CAMAC Dataway under CAMAC control or reconstructs the analog signal in any channel for display on a lab scope. Other circuitry on the board permits reading the settings of the front panel switches as a digital code on the CAMAC Dataway.

In the following detailed functional description of the instrument we will discuss the operation of the two boards separately, and each board will be divided in several logical subsections. A block diagram, timing diagrams, and a schematic of the controller board are found at the end of this section to help clarify the test and to aid in trouble shooting and repair.

5b. ADC Board

1. General Description: The analog to digital converter in the Model 2264 is a two stage parallel-serial type converter. The four most significant bits (MSB's) are obtained from a flash converter consisting of 15 high speed comparators whose outputs are reduced to binary form by a fast encoder. The binary (MSB) outputs are then fed into an output latch and into the inputs of a high speed 4 bit DAC. A signal proportional to the difference between the DAC output and the input signal is constructed by a fast difference amplifier. This difference signal is then digitized by another 4 bit flash converter. The encoded outputs of the second converter are the least significant bits (LSB's) of the ADC.

In front of the ADC is a fast track and hold circuit with a well defined aperature time (aperature jitter ±25 psec) which presents fixed voltage samples of the ADC for digitization eliminating slewing problems in the comparators.

2. Track and Hold Circuit: The track and hold circuit consists of a balanced diode sampling gate which is switched by a fast comparator in conjunction with a differential pair providing proper voltage and current inputs to the diode bridge switch. The output of the gate is connected to a unity gain high speed discrete amplifier, which is basically a differential cascode amplifier with a complimentary symmetry push-pull output. When the gate is open the amplifier tracks the input signal and the instantaneous output voltage is imposed on a small hold capacitor. When the gate is closed, the signal is held at the level stored on the capacitor. Input bias current is

provided by a pair of thermally compensating PNP transistors which also compensate for capacitor leakage.

In operation the circuit tracks until a convert command (ADC strobe) pulse is received, during which time it is able to acquire a full scale voltage change. It then goes into a hold state for 50 nsec. About 20 nsec of that time is allowed for switching transients to delay and for the output voltage to settle to within a half LSB of its final value. The output of the track and hold is connected directly to the input of the first comparator chain. The 3 dB bandwidth for a full scale voltage change is 30 MHz.

3. ADC: The first 15 comparators have their switching levels set at 320 mV intervals between ±2.560 volts by a resistor chain and precision regulated bias voltages. As soon as the track and hold output has settled the comparators are latched into states corresponding to their biasing and the signal level. The complementary outputs of the comparators feed a series of NOR gates whose outputs are wired ORed together. This gives a 4 bit binary output which is latched into an output register. The 4 bit binary signal is also applied to a DAC consisting of precision current sources and fast current switches. The DAC converts the 4 MSB's into an analog current which is applied to the summing node of a fast discrete op amp similar to the one used in the track and hold circuit. At the same time a current proportional to the input signal is applied to the summing node. The input currents to the node are of such a polarity that the op amp output is proportional to the difference between the DAC output and the input signal. The output of the subtractor op amp is then applied to another 4 bit flash converter like the one used to obtain the 4 MSB's but biased to fit the difference output voltage range of the subtractor. In order for this difference signal to lie in the proper range, the DAC gain and offset must be precisely adjusted. The LSB comparators are briefly unlatched and allowed to switch to states determined by the difference signal and their bias level; then they are latched into these states and decoded. This second converter then yields the 4 LSB of the 8 bit output. The LSB's are fed directly to the output cable from the decoders.

5c. Controller Board

General description - refer to first paragraph in the functional description section.

Analog Multiplexer: This section of the controller multiplexes the signals from up to 8 different analog signal sources into the input of the ADC board and strobes the resulting digitized data into a FIFO buffer from which the data is later strobed into 8800 memory modules.

The input for each of the eight channels to the multiplexer is through an inverting op amp (LM318) with input resistor and feedback resistors selcted to give the desired input resistance and the gain required to translate the

input voltage range into the -2.56 V to +2.56 V ADC range. Another resistor connected to the summing node of each amplifier and by front panel switch to either a -12 V, 0 V, or +12 V to produce an amplifier output of either +2.56 V, or -2.56V so that a unipolar input voltage range can be translated into the bipolar ADC range.

The outputs of the eight amplifiers are multiplexed through two quad DMOS FET switches (SD5001's) into the summing node of a unity gain fast-settling inverting op amp (Q6-Q12). The output of this amplifier drives the input to the track and hold circuit on the ADC board.

The gate pulses for the FET switches come from the stages of a recirculating shift register (74LS74, 74LS174, 74S153), which together with a 5 MHz gated oscillator, two univibrators (74LS221), a reset flip-flop (74S112) and some NOR gates forms a programmable burst clock. The number of stages included in the shift-register loop and therefore the number of channels multiplexed into the ADC is controlled by input from the front panel "Input Channels" switch to the 74S153 data selector. The burst clock produces the ADC convert command pulses and the parallel load pulses for the resulting digital data going into the FIFO's (9403's). The burst-clock is turned on by the negative edges of pulses from the master clock which controls the sampling rate/channel. It is turned off by a reset pulse from the programmable shift register. For more detail see the Multiplexer-ADC timing diagram at the end of this section.

Master CLK: The Master CLK pulses come from a digital multiplexer (74S151) which multiplexes several gates of different frequencies from the outputs of a divider (74LS390) clocked by a 4 MHz crystal oscillator. An input from an external connector may also be selected by the 74S151 multiplexer for external control of the sampling rate. The 74S151 is programmed by the sampling rate switch on the front panel.

Memory Strobe and Refresh Generator: After data has been entered into the FIFO's (9403's) it bubbles through toward the FIFO output register. Status signals from the FIFO output and clock signals from a 5 MHz oscillator (74LS324) then control the shifting of the data out of the FIFO's onto the memory datalines in synch with memory strobe pulses. This control is accomplished by the memory strobe and refresh pulse generator logic block (IC's located in sockets GD, GE, GF, GG, GH, and FH). This logic generates refresh pulses about every 10 usec and ensures that memory strobe pulses and refresh pulses do not overlap and are properly timed with respect to one another. (See Model 8800 manual for detailed timing diagrams).

Stop Conversion and Memory Read Control Logic: When a stop trigger or CAMAC F(25) command is received a programmable counter (¼74LS279 and 4 74LS161's) is enable having been loaded at the beginning of the conversion period with a count determined by the settings of the post-trigger samples switch and the positions of jumpers on the platform located in socket AO (see section on jumper option programming). At this time the clock for the counter is the master sampling clock. After the selected number of post-trigger samples, the counter reaches full count, resets itself and sends a pulse to the memory read control logic block (IC's located in sockets DH, EH, EG, DG, DF, FG, DJ, DK, EF). This logic block disables the Master Clock multiplexer (74S151). It allows time for data from the last samples to be transferred from the FIFO to the 8800 memory. Then it causes the memory R/W line to go low (Read Mode) and transfers control of the memory strobe and refresh generator from the output registers of the write FIFO's (9403's) to the input register status signals of the Read FIFO's (3351l's). At this time a mono-stable (½74LS221) is enabled which strobes data into the read DIDO's in sync with the memory strobe pulses. Data now being read out of the memory passes through a buffer latch (74LS374) and is demultiplexed into odd and even data words into the two read FIFO's. Odd numbered data words filter through FIFO #1 (DJ) and even numbered data words bubble through FIFO #2 (DK). A "first word" flag is entered on the 9th bit line of FIFO #1 when the first 8 bit data words enters on the other 8 lines. The programmable counter is now clocked by a signal from the memory read control logic and acts as a memory read cycle counter. After enough cycles have occurred to read all of the memory, the counter resets. The first word flag is raised again, and the read process may repeat again. Programming jumpers on a platform in socked CK allow programming the counter for 32K, 64K, 96K, or 238K words (1K = 1024).

Data Display/CAMAC Readout Control: This section controls the readout of the data from the Read FIFO's and selects the data words to be latched into the DAC input register and the tristate buffer registers which output to the CAMAC dataway. As soon as the first word flag and first data word pair appear at output registers of the read FIFO's the internal logic is set-up to begin readout. Readout may proceed in a continuous cyclic mode or in a interrupted single memory scan under control of CAMAC F(2) read commands depending on the state of the CAMAC ENABLE line. If this line is low the readout will be under control of the FIFO's and Readout control logic alone and will proceed automatically at a rate depending on FIFO timing and the timing of monostables inside the readout control section itself. This is the data display mode used when data is to be converted to analog form and displayed on a scope through the on board DAC (DAC-08) and DAC output current-to-voltage amplifier (LM318 and 2N2368A). A scope trigger pulse is initiated when the first word flag is up so that the display sweep may be triggered at the earliest sample in the data.

Selection of the channel to be displayed is done by (1) the 2^0 display channel switch input to the multiplexing DAC input register. This decides whether odd or even data is latched into the register and (2) the programmable sequencer made up of a 9319 (BG), a 74LS151(BF), a 74LS367(CE), a 74LS173(CD), a 74LS74(CG) and other logic gates. This circuitry decides at the beginning of a read cycle how many data word pairs are skipped before a latch pulse is sent to the output registers. It does this on the basis of input data from the 2^1 and 2^2 terminals of the "Display Channel" switch of CAMAC A1, A2 information latched into the 74LS173 by an F(16)·S2 command when CAMAC controlled readout is to be done. After this initial positioning of the first latch pulse at the first word of the channel to be displayed, the circuitry decides how many word pairs are to be skipped before another latch pulse is produced. It does this on the basis of input from the "Input Channels" switch. For example, in the single and two channel mode no word pairs are skipped, in the four channel mode one word pair is skipped and in the eight channel mode three word pairs are skipped between latch pulses.

When the CAMAC ENABLE line is set high by an F(26) command, a LAM will be raised when the first word flag and first word pair appears at the FIFO output registers. Now an F(16)·S1 pulse latches A1, A2 information in the 74LS173 to determine which channels are to be read (see previous paragraph). F(16)·S2 starts the normal readout process discussed before and the first desire word pair is latched into the output latches and readout proceeds until the next word pair from the selected channels appears but no latch pulse is produced and readout stops until the first word has been placed on the CAMAC data lines by an F(2) command which enables the register output. The next word pair is then latched into the register on the trailing edge of the F(2)·S2 pulse and readout proceeds until the next word pair appears at the register inputs but again halts until another F(2)·S2 releases the previous word to the dataway and then latches this next word into the register and restarts the readout. Readout proceeds in this fashion until the first word flag and the accompanying word pair appear again, at which time readout stops until another F(16) is received. If an F(24) command is issued the CAMAC ENABLE line goes low, the LAM is disabled and the F(16) command will reset the logic into the data display mode.

CAMAC Control Logic: This section uses 74LS154(DL) and some other logic gates to decode the CAMAC function lines and generate the CAMAC control and response signals. For a complete description of these commands and responses see the CAMAC command and function code section of the data sheet and the CAMAC command sequence on page 4.4.

Memory Enable Control: This circuitry is included on chips located in sockets FF (¼74L279) and DD (¼74S08). The initiate pulse sets the Memory Enable line low enabling the first memory in the chain connected to the 2264. The line returns high when the first memory strobe pulse occurs (enabling is done by high to low transition). When the last memory is full a memory enable return pulse is sent back to the controller and causes the memory enable line to go low reenabling the first memory again. For more details see the Model 8800 manual.

Auxiliary and Monitoring Circuitry: Allows digital codes associated with each front panel switch (except "display channel" switch) to be gated onto the CAMAC dataway by appropriate CAMAC commands through tristate buffers (74LS 240A) located in sockets EL, EM, and EN.

A 7485 (BM) monitors the states of the "sample rate" and "input channels" switch and raises a flag if the sample rate is too high for the number of channels. This condition also enables an astable multivibrator 555 (AM) which blinks a warning LED on the front panel.

Another 7485(CL) monitors the "display channel" switch and "input channels" switch and disables the display DAC if the "display channel" switch is set to a channel which does not have its input switched into the multiplexer as determined by the setting of the "Input Channels" switch.

A +12 voltage regulator (1N758, LM301, Q14) supplies a +12 V reference to the input offset switches and a -12 V regulator (LM301, Q13) which supplies the -12 V reference to the input offset switch and the -12 V operating voltage for the 33511 read FIFO's. These two regulators also supply the +12 V and -12 V reference and operating voltages to the display DAC (DAC-08).

A separate +12 V regulator (78MG) supplies the +12 V operating voltage for the multiplexer op amp (Q6-Q12).

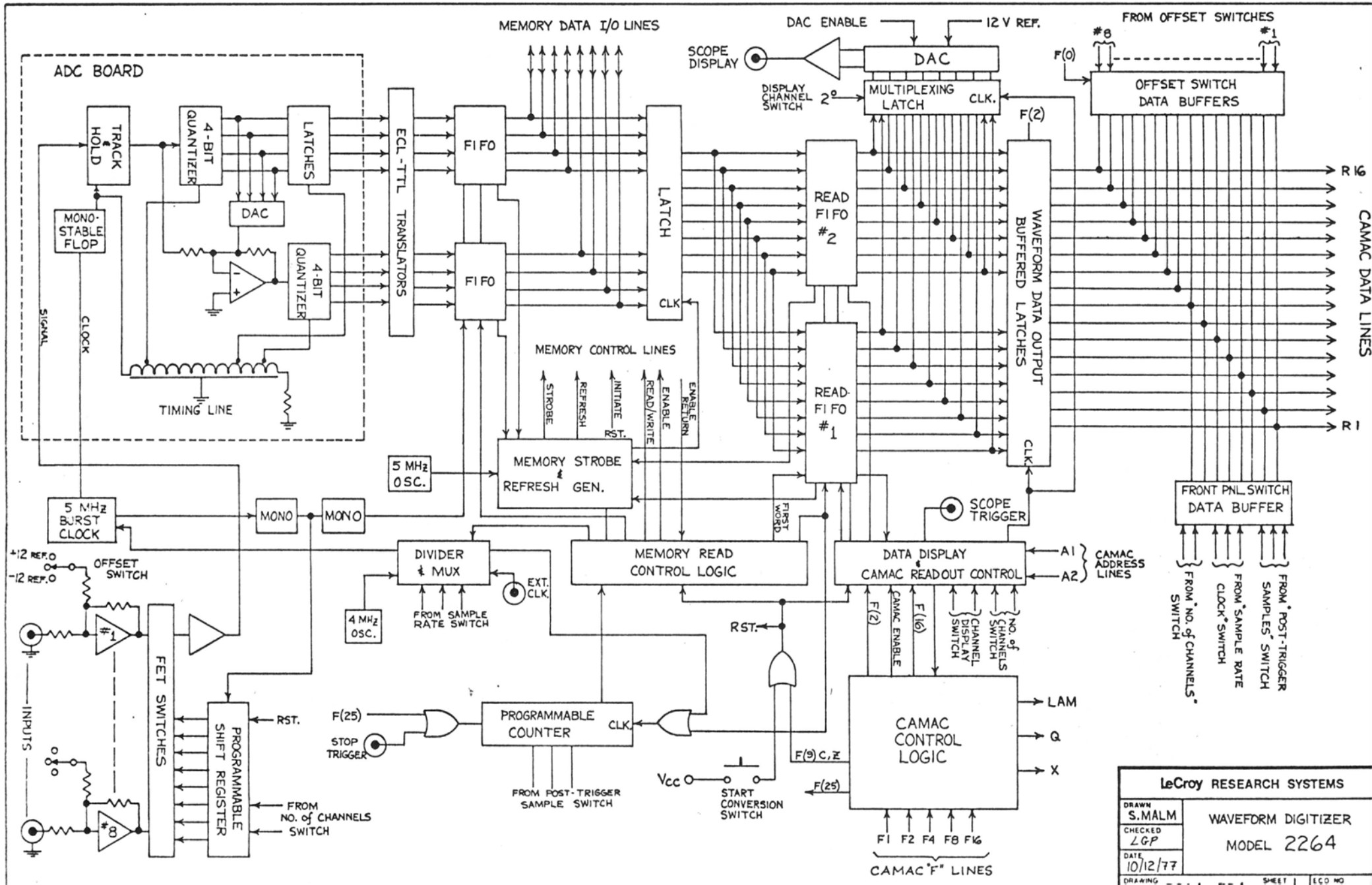
Jumper Option Programming of the 2264

The 2264 may be programmed to operate with 1, 2, 3 or 4 associated Model 8800/8 memory modules connected in tandem. Also, the post-trigger samples counter may be programmed so that the front panel post-trigger samples switch indicates either increments of 1024 or 2048 post-trigger samples. The programming is done by jumpers located on sockets CK and AO on the controller board.

The following table indicates which pins have jumpers between them on each socket for each of the possible options.

# of 8800's	Jumpers Socket AO	Jumpers Socket CK
1	1 - 13, 2 - 12	1 - 16
2	1 - 13, 3 - 12	2 - 15
3	14 - 13, 2 - 12	3 - 14
4	12 - 13 - 14	4 - 13

Post-Trigger Switch Increments	Jumpers Socket AO
1024	6-8, 5-9, 4-10, 3-11
2048	7-8, 6-8, 5-10, 4-11



LeCroy RESEARCH SYSTEMS	
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CHECKED LGP	MODEL 2264
DATE 10/12/77	
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